OTTO VON GUERICKE UNIVERSITÄT MAGDEBURG
EIT FACULTY OF ELECTRICAL ENGINEERING AND INFORMATION TECHNOLOGY

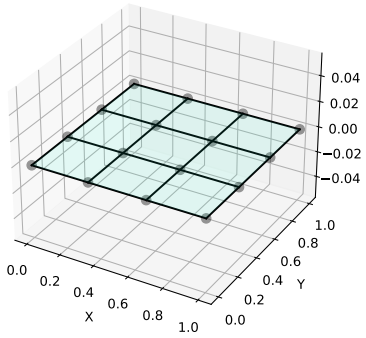
Hardware-Oriented Technical Computer Science

Modeling and Verifying of 3D Network-on-Chip Benchmarks for the RatatoskrM3D Simulator

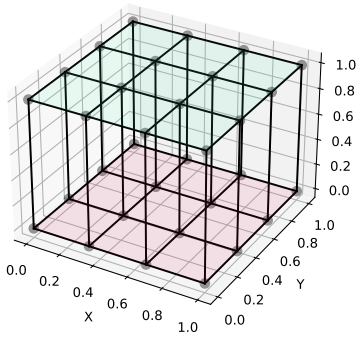
Research Project or Bachelor/Master Thesis

Research field

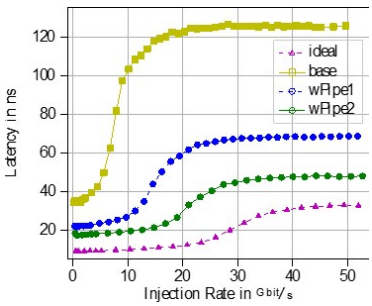
Network-on-Chips (NoC) are widely used in multi-core System-on-Chips (SoC) as the communication backbone, replacing standard bus architectures. NoCs are inspired by the Internet network, which has a packet-based message transfer and routers to connect nodes. 3D System-on-Chips benefit from several advantages such as smaller chip area and shorter interconnects between components. For these systems, classic 2D NoCs can be extended to the third dimension. Simulators can be used to examine the resulting challenges and constraints and to explore the design space quickly and easily.



2D NoC



3D NoC



Simulation Results

Research topic and working hypothesis

The student shall address the question of how to extend the existing benchmarks for the RatatoskrM3D simulator developed at this chair in order to obtain more realistic simulation results. First, the existing synthetic benchmark is to be adapted so that it is also suitable for heterogeneous 3D NoCs with multiple clock domains. Furthermore, simulation results are available for the same 3D NoC model created with other simulators. Based on these results, a new similar benchmark shall be created and the results of the simulators shall be compared.

Work plan

- Adapt synthetic benchmark for RatatoskrM3D
- Evaluate simulation results of other simulators
- Implement new benchmark
- Compare results of RatatoskrM3D and other simulators

Skills

Required:

- Very good knowledge of C++17

Desired:

- Basic knowledge of SystemC
- Advanced understanding of NoCs

Contact

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SCAN ME

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